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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,629	03/03/2004	Soo-Chan Lee	2421-000033/US	3096

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,629	LEE ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *11-32,38 and 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 33-37 and 40-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Invention I, claims 1-10, 33-37 and 40-42 in the reply filed on January 24, 2006 is acknowledged. The traversal is on the ground(s) that "the search and examination of an entire application can be made without a serious burden". This is not found persuasive because even though they are classified together, each invention can be shown to have formed a separate subject for inventive effort when the examiner can show recognition of separate inventive effort by inventors. For example, as stated in the restriction, Invention I has separate utility such as a stacker for stacking devices before and after a test as well as a robot and Invention II has separate utility such as a socket assembly having a socket block and plurality of socket guides as well as a lead pusher assembly.

The requirement is still deemed proper and is therefore made FINAL.

2. Claims 11-32 and 38-39 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on January 24, 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-10, 33-37 and 40-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al (6384593).

Regarding claim 1, Kobayashi et al disclose [see Figs. 1-2] a semiconductor device test apparatus comprising a main body (combination of sections 200, 300 and 400); a soak chamber (temperature chamber 101), a test chamber (102); a desoak chamber (temperature stress removing chamber 103); wherein the soak chamber (101), the test chamber (102), and the desoak chamber (103) can be separated from the main body (200, 300, and 400).

Regarding claim 2, Kobayashi et al disclose the soak chamber (101), the test chamber (102), and the desoak chamber (103) can be separated from the main body (200, 300 and 400) using a sliding unit.

Regarding claim 3, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of sections 200, 300 and 400); and a stacker (transfer means 304 and 404) for stacking devices (ICs) before and after a test, the stacker (304 and 404) including user trays (test trays TST) for stacking the devices (ICs), the user trays (TST) interchangeable such that the user trays (TST) may be being used to stack the devices (ICs) prior to the test and to stack the devices (ICs) after the test.

Regarding claim 4, Kobayashi et al disclose the user trays (TST) are interchanged in accordance with the process of the test.

Regarding claim 5, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of section 200, 300 and 400); a stacker (transfer means 304 and 404) for stacking devices (ICs) before and after a test, the stacker (304 and 404) including at least one user tray feeder (means 304) predesignated with a function for stacking un-

tested devices (ICs) and at least one user tray sender (means 404) predesignated with a function, for stacking tested devices (ICs), the user tray (test tray TST) functions being interchangeable during stacker operation.

Regarding claim 6, Kobayashi et al disclose a semiconductor device test apparatus comprising: a main body (combination of sections 200, 300 and 400); and a stacker (transfer means 304 and 404) arranged in the main body (200, 300 and 400), the stacker (304 and 404) having a user tray feeder (means 304) which loads a plurality of user trays (test TST) having a desired quantity of devices (ICs) to be tested and a user tray sender (means 404) which loads the plurality of user trays (TST) having the devices sorted by their grades in accordance with the test result, the user tray feeder (304) and the user tray sender (404) being interchanged in their uses in accordance with the process of the test.

Regarding claim 7, Kobayashi et al disclose a soak chamber (temperature chamber 101) for receiving the test tray (TST) inputted from the device loader (loader section 300), and for preheating or precooling the devices (ICs); a test chamber (102) for connecting the preheated devices (ICs) in the soak chamber (101) to a socket of a test head (tester head 104) and for performing a test; a desoak chamber (stress removing chamber 103) for receiving the test tray (TST) discharged from the test chamber (102) and for discharging them to a device unloader (unloader section 400) after recovering them to a room temperature, wherein the soak chamber (101), the test chamber (102) and the desoak chamber (103) can be separated from the main body (200, 300 and 400) using a sliding unit.

Regarding claim 8, Kobayashi et al disclose the soak chamber (101) and the test chamber (102) are made of one body (chamber section 100) to be separated in the same direction.

Regarding claim 9, Kobayashi et al disclose the desoak chamber (103) is able to be separated in same direction as the separation direction of the soak chamber (101) and the test chamber (102).

Regarding claim 10, Kobayashi et al disclose a loading robot (movable head 303 and movable arm 302) for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (304) and mounting them on a test tray (TST) being on a device loading stage (300); a sorting robot (movable head 403) for picking up the device discharged to the device unloader (400) and for carrying them to a plurality of sorter tables (storage rack 201) in accordance with the test result; and an unloading robot (movable arm 402) for picking up the device carried to the sorter table (201) and for carrying them to the user tray sender (404).

Regarding claim 33, Kobayashi et al disclose a semiconductor device test apparatus comprising a loading robot (movable head 303 and movable arm 302) for picking up devices (ICs) to be tested, which are in a stand-by status in the user tray feeder (304) and mounting them on a test tray (TST) being on a device loading stage (300); a sorting robot (movable head 403) for picking up the device discharged to the device unloader (400) and for carrying them to a plurality of sorter tables (storage rack 201) in accordance with the test result; and an unloading robot (movable arm 402) for picking up the device carried to the sorter table (201) and for carrying them to the user tray sender (404) wherein the operating speed of the loading robot (302 and 303), the sorting robot (403) and the unloading robot (402) is determined based on the speed of testing the device (ICs).

Regarding claim 34, Kobayashi et al disclose at least one robot (304) used in a test that receives control signals instructing the at least one robot (302 and 303) to carry a device (ICs) at a calculated speed, the calculated speed corresponding based on a time of test execution.

Regarding claim 35, Kobayashi et al disclose a method for constructing a semiconductor device test apparatus comprising: attaching, during manufacture, a soak chamber (101), a test chamber (102), and a desoak chamber (103) to a main body (200, 300 and 400) so that the soak chamber (101), the test chamber (102), and the desoak chamber (103), may be later separated.

Regarding claim 36, Kobayashi et al disclose creating the soak chamber (101), the test chamber (102), and the desoak chamber (103) with attachment configurations, the attachment configurations used to attach the soak chamber (101), the test chamber (102), and the desoak chamber (103) with the main body (200, 300 and 400).

Regarding claim 37, Kobayashi et al disclose a method for stacking devices (ICs) in a semiconductor test apparatus comprising, predesignating at least one user tray feeder (means 304) for stacking un-tested devices, predesignating at least one user tray sender (means 404) for stacking tested devices, designating at least one user tray feeder (304) for stacking tested devices based on the test; stacking at least one tested device (ICs) on the at least one user tray feeder (304).

Regarding claim 40, Kobayashi et al disclose a method for controlling a robot speed of a semiconductor device test apparatus, comprising the steps of: sending control signals to at least one robot (means 304) to carry a device (ICs) for a test detecting a time for the test; calculating a desired speed value of the robot (304) corresponding to the test time detected, and informing the corresponding robot (304) of the calculated speed value to control the speed of the robot (304).

Regarding claim 41, Kobayashi et al disclose the time for the test begins when the device (ICs) contacts a test head (tester head 104) and ends when the device (ICs) is released from the socket.

Regarding claim 42, Kobayashi et al disclose the step of detecting the time for the test includes retrieving stored values of pretested, like kind devices.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. [See PTO-892 for further details].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:30 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (517) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
April 6, 2006